In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An integrated circuit component comprising:

logic capable of being configured to interface with a first portion of a system bus, wherein the first portion of the system bus comprises only approximately half of a set of signal lines that comprise ~~a first plurality of signal lines of the system bus, but not all of the signal lines of the~~ system bus; and

logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus, wherein the second portion of the signal bus comprises a remaining portion of the system bus not included in the first portion, wherein the logic capable of being configured to interface with the first portion of the system bus is operatively connected with the logic capable of being configured to interface with the companion integrated circuit ~~a second plurality of signal lines of the system bus, which are not a part of the first plurality of signal lines~~.

2. (Original) The integrated circuit component of claim 1, further including link layer control logic in both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the

companion integrated circuit, the link layer control logic being configured to exchange link layer control information, such that both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit possess complete link layer control information for the data being communicated over the system bus.

3. (Original) The integrated circuit component of claim 1, further including a programmable delay buffer in both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit, wherein the respective programmable delay buffers are configured with differing delays so that communications from the integrated circuit component with the system bus are synchronized with communications from the companion integrated circuit and the system bus.

4. (Original) The integrated circuit component of claim 1, further comprising unified bus logic configured to consolidate information received from both logic elements.

5. (Original) The integrated circuit component of claim 1, further comprising functional logic for performing at least one logic operation for the integrated circuit component.

6. (Original) The integrated circuit component of claim 1, wherein the system bus is a point-to-point serial communication bus.

7. (Original) The integrated circuit component of claim 5, wherein the functional logic performs the logic operation of a memory controller.

8. (Original) The integrated circuit component of claim 1, further comprising logic capable of configuring the integrated circuit component for operation with a companion integrated circuit component.

9. (Original) The integrated circuit component of claim 1, further comprising logic capable of configuring the integrated circuit component for operation in a stand-alone configuration.

10. (Original) The integrated circuit component of claim 1, wherein the first portion of the system bus is substantially one-half of the system bus.

11. (Currently amended) A system comprising:

a plurality of companion integrated circuit components that collectively implement a logic function embodied in a single, conventional integrated circuit component, each companion integrated circuit component comprising:

a first logic interface for communicating with a remote component via a portion of a system bus, wherein the portion of the system bus comprises only

approximately half of a set of signal lines that comprise a ~~plurality of signal of signal lines of the system bus, but not all of the signal lines of~~ the system bus;

a second logic interface for communication with a companion logic interface of a remaining one of the plurality of the integrated circuit components over a separate bus, wherein the first logic interface is operatively connected with the second logic interface; and

logic for controlling the selective communication of information received by the first logic interface via the portion of the system bus through the second logic interface to the companion integrated circuit.

12. (Previously presented) The system of claim 11, wherein the logic for controlling the selective communication of information received from the first logic interface through the second logic interface further includes first split bus logic configured to interface with the first logic interface, and second split bus logic configured to interface with the second logic interface.

13. (Original) The system of claim 12, further including link layer control logic in both first split bus logic and the second split bus logic, the link layer control logic being configured to exchange link layer control information, such that both the first split bus logic and the second split bus logic possess complete link layer control information for the data being communicated over the system bus.

14. (Original) The system of claim 12, further including a programmable delay buffer in both the first split bus logic and the second split bus logic, wherein the respective programmable delay buffers are configured with differing delays so that communications between the integrated circuit components and their respective portions of the system bus are synchronized.

15. (Original) The system of claim 11, further comprising functional logic that performs a conventional functional operation.

16. (Original) The system of claim 11, wherein the functional logic comprises a memory controller.

17. (Original) The system of claim 16, further comprising integrated circuit memory components in communication with the memory controller.

18. (Original) The integrated circuit component of claim 11, further comprising logic capable of configuring the integrated circuit component for operation with a companion integrated circuit component.

19. (Original) The integrated circuit component of claim 11, further comprising logic capable of configuring the integrated circuit component for operation in a stand-alone configuration.

20. (Currently amended) An integrated circuit component comprising:

a first set of conductive pins for channeling communications with a remote component via only a portion of a system bus, wherein the portion of the system bus comprises a plurality of signal lines ~~of the~~ that make up a system bus, but not all of the signal lines ~~of the~~ that make up the system bus;

a second set of conductive pins for channeling communications with a companion integrated circuit component;

additional conductive pins for carrying additional control and communication signals;

wherein collectively, the conductive pins of the integrated circuit component do not directly accommodate all ~~signals~~ signal lines of the system bus, but rather directly accommodate fewer than all of the signal lines of the system bus.

21. (Original) The system of claim 20, wherein each integrated circuit component further comprises a logic interface for communicating with a remote component via the first set of conductive pins.

22. (Original) The system of claim 21, wherein each integrated circuit component further comprises a logic interface for communication with the companion integrated circuit component via the second set of conductive pins.

23. (Original) The system of claim 20, wherein the integrated circuit component further comprises functional logic for performing a conventional logic operation.

24. (Original) The system of claim 20, wherein functional logic is interfaced to a remote integrated circuit component through a third set of conductive pins.